

# Highlights

Electronic and thermal transport from the nanoscale to the macroscale - 2019

## A WSe<sub>2</sub> vertical field emission transistor

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The recent observation of metallic edges in atomically thin WSe<sub>2</sub> monolayers grown by CVD, the lower bandgap (~1.6 vs. ~1.8 eV), effective electron mass (0.33 vs. 0.57 m<sub>0</sub>, the rest mass of the electron) and electron affinity (~3.9 vs. ~4.2 eV) would suggest that WSe<sub>2</sub> is a far better field emitter than MoS<sub>2</sub>. In this paper, we use CVD to fabricate monolayer and few-layer WSe<sub>2</sub> flakes on a SiO<sub>2</sub>/Si substrate and investigate their electrical properties, under high vacuum, using back-gated transistor structures. We show that the WSe<sub>2</sub> flakes, contacted by Ni, exhibit n-type conduction, with conductivity highly controlled by the back-gate voltage. Taking advantage of the gate-controlled n-type doping, we locally probe the field effect (FE) current from a monolayer WSe<sub>2</sub> and we achieve a FE current in the range of μA from the flat part of the flake. More importantly, we demonstrate that the FE current can be modulated by the back-gate voltage, thus realizing the first vertical FE transistor based on a WSe<sub>2</sub> monolayer. We unveil the physics mechanisms underlying the operation of such a device and give indications for its optimization to enhance its driving current capability and to lower the applied voltage. This study can pave the way to the further exploitation of WSe<sub>2</sub> in a new generation of devices for vacuum electronics.

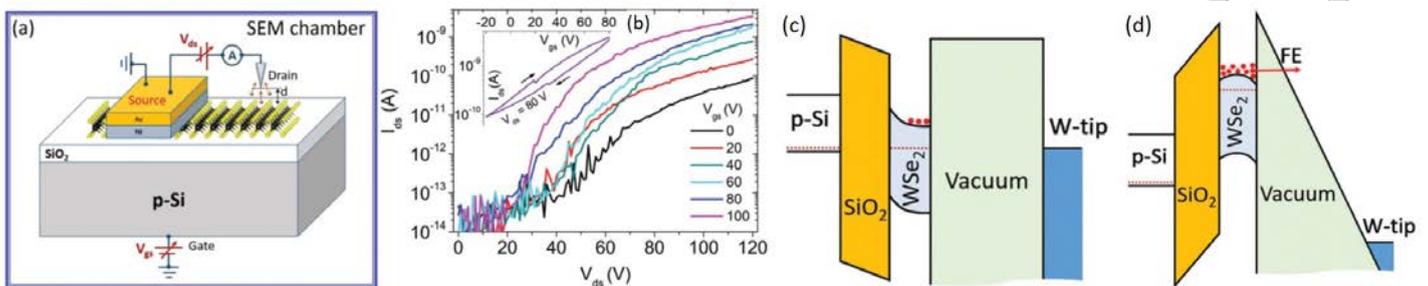


Fig. 1: (a) Layout of a back-gate FE transistor with a WSe<sub>2</sub> monolayer channel over a SiO<sub>2</sub>/Si substrate. The W-tip labelled as the drain, which collects field emitted electrons and monitors the current, is kept at a distance d from the sample, while the voltage is ramped up. (b) FE current measured at given back-gate voltages (V<sub>ds</sub> steps of 1 V). (c) Band diagram for (c) the unbiased device and for (d) the device under V<sub>ds</sub> > V<sub>gs</sub> > 0 V bias conditions.